

Remarks

The Final Office Action dated April 14, 2010 notes that the drawings and the specification are objected to, and maintains the following rejections: claims 1-2, 4-9 and 12-14 stand rejected under § 103(a) over the Krakauer '283 reference in view of the Chin '602 reference; claim 10 stands rejected under § 103(a) over the '283 and '602 references in view of the Ker '615 reference; claims 11 and 15 stand rejected under § 103(a) over the '283 and '602 references in view of the Lai '022 reference; claims 1-2, 4-9 and 11-15 stand rejected under § 103(a) over John (U.S. Patent No. 6,522,511) in view of Ker (U.S. Patent No. 6,912,109); and claim 10 stands rejected under § 103(a) over the '615 reference, although because such a rejection would be *prima facie* improper on its face (e.g., no correspondence via Ker), Applicant presumes that this rejection is intending to mean rejected over John (U.S. Patent No. 6,522,511) in view of Ker (U.S. Patent No. 6,912,109) and further in view of the '615. Applicant traverses all of the rejections (including the improper Ker-based rejection of claim 10) and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses each of the rejections for numerous reasons. First, the § 103(a) rejections based on the '283 reference are entirely illogical and improper § 103(a) rejections because the cited references not only teach away from the Office Action's proposed combination but violate the § 103(a) mandate set forth in M.P.E.P. § 2143.01. In essence, the Examiner's rejection argues that the skilled artisan would be led to modify Figure 2 of the '283 reference by placing a generic resistor in series with a specially-designed resistor (dealing with the main purpose of the '283 reference) to protect the specially-designed resistor from a problem that is nonexistent according to the '283 reference. Attempting to align Applicant's claims with unrelated teachings of these references, the Examiner improperly refers to specially-designed resistor 42 as a "diode" and construes the "diode" as the alleged "capacitive device", and then attempts to design a non-workable circuit by modifying Figure 2 of the '283 reference without any consideration to the central purpose of the '283 reference and its specially-designed resistor.

A careful reading of the '283 reference would reveal that its entire disclosure is based on use of a modulation control device which operates in parallel with a clamping

device to provide most-immediate protection in terms of both the lowest level of detected ESD voltage spike and the fastest time possible. The discussion of the advantage of achieving the lowest level of detected ESD voltage spike begins at Col. 2:31-35, includes the discussions of Figures 2 and 4, as well as the timing diagram of Figure 3, and continues throughout the disclosure in connection with the parallel operation of the modulation control device and the clamping device. The importance of providing immediate protection as fast as possible is perhaps most emphasized via the '283 reference at Col. 6:18-26 ("to be effective ... [and] ensure such operation, resistor 42 is designed to have a channel width/length ratio ..." for the voltage activation threshold and related response time). By placing a generic resistor in series with the specially-designed resistor 42, the Examiner significantly increases the resistance value and adversely delays the reaction time of the modulation circuit, significantly increases the threshold trigger value at which the modulation control device activates for the clamping device resistance, and destroys the noted importance of having the resistor 42 designed to have its specific channel width/length ratio for the voltage activation threshold and related response time. Accordingly, in an improper hindsight attempt to redesign Figure 2 of the '283 reference, the Examiner not only overlooks the '283 reference's teaching of the specially-designed resistor but, by placing a generic resistor in series with the specially-designed resistor, eviscerates its special design and alleged special operation.

The illogical of the rejection is further apparent as the '283 reference explains its core teachings in connection with the related embodiments of Figures 2 and 4. Each of Figures 2 and 4 includes the specially-designed resistor (42 (Fig. 2) and 72 (Fig. 4)) "constructed from a PMOS transistor which has its gate coupled to its respective drain" ('283 reference at Col. 4:38-41), as is conventional for a resistor implemented in ICs. Thus, the Examiner apparently also argues that a skilled artisan would modify these figures to include a (generically-designed) resistor as taught in the '602 reference, presumably constructed in the same manner as the specially-designed resistor (42/72) in order to protect the specially-designed resistor. Disadvantageously, without a further modification to include an ESD-protection circuit for the similarly-constructed generically-designed resistor, any protection from an ESD spike that would be

attributable to inclusion of the generically-designed resistor would be undermined by the same ESD spike destroying the similarly-constructed generically-designed resistor.

Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('283) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). ("[W]hen the prior art teaches away from combining certain known elements...."). Applicant submits that the combination would render the invention inoperable because the addition of the resistor as asserted by the Office Action would increase the delay time (before the ESD clamp device 18 of the '283 reference turns on) in a manner that is expressly avoided by the '283 reference. This would inhibit the ability of the circuit to turn on the clamp device "before any damaging currents and/or voltages are experienced by I/O pad 12." Col. 6:21-22 of the '283 reference. The '283 reference discloses that the "resistor 42 is designed to . . . maintain a proper voltage divider relationship with the diode stack 46 while also providing adequate AC response time for ESD events." Col. 6:23-25. The addition of a resistor R2' in series with asserted capacitive device 42 would change the AC response time for ESD events, as well as the voltage divider relationship between the diode stack 46 and the device 42. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

Further, the Office Action has failed to provide proper motivation for the asserted hypothetical embodiment. M.P.E.P. §§2142 and 2143.01 require that the Office Action must provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn* , 441 F.3d 977, 988 (Fed. Cir. 2006). The Office Action asserts that it would have been obvious "to provide a resistor in series with the capacitive device [42 of the '283 reference], to protect the MOS transistor by providing current limiting means between the pad and the transistor, and the '602 reference teaches that a resistor connected in series with a diode connected MOS transistor to protect the transistor." Office Action page 4. However, the MOS transistor of the '602 reference is used as a clamping device, not as a time delay as the transistor of the '283 reference is asserted to be. One of skill in the art would understand that the

electrical conditions each transistor is exposed to are different. Accordingly, one of skill in the art would not look to such teachings to solve a problem regarding protection of a specific device of an ESD protection circuit where it is clear that neither the specific device nor the ESD protection circuit presents no need for such protection. For at least these reasons the Office Action has failed to present a *prima facie* and/or sustainable case of obviousness. Accordingly, the § 103 rejections based on the '283 reference and the '602 reference are improper and should be withdrawn.

Applicant further traverses the § 103(a) rejection of claim 10 over the Ker '109 reference for the same reasons presented above and further because, to the extent this combination is explained and understood, the asserted modification based on the '109 reference would be using a thyristor which would further undermine the previously-discussed purpose and operation of the primary '283 reference (alone or with the '602 reference) and the resultant hypothetical embodiment would still not correspond for the reasons presented above.

Applicant further traverses the § 103(a) rejections based on the cited Krakauer '283 reference because the '283 reference, either alone or in combination with the other cited references, lacks correspondence to the claimed invention. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.*, a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. Further, as discussed above, the Examiner's rejection is based on misreadings of the claimed invention as a whole and the prior art as a whole (*e.g.*, with the misuse of the "diode", "capacitive device" and "resistor" language). Because none of the cited references teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejections fail.

More specifically regarding the time-delay circuit that includes a resistor and a capacitive device connected as in the claimed invention, the Office Action acknowledges that the '283 reference does not teach or suggest such a time-delay circuit that includes a resistor and a capacitive device as so connected (*see, e.g.*, page 4 of the instant Office Action). The '602 reference, however, also fails to teach such a time-delay circuit. The asserted resistor R2' and MOS transistor T1 are not part of a time delay circuit in the '602

reference. Instead, the transistor T1 is disclosed as a clamping device. *See* Col. 3:38-40 of the '602 reference. Further, the asserted resistor R2' and the asserted transistor T1 are not connected in series between pad 110 and any other transistor. Rather, the asserted resistor R2' and the asserted transistor T1 are connected in series between the pad 110 and a reference voltage Vss. Moreover, the '602 reference teaches a delay circuit that does not include the asserted resistor R2' or the asserted transistor T1. Instead, the delay stage is disclosed as including resistance r2 and c4. *See* Col. 3:56-58 of the '602 reference. However, the resistor and capacitor of the delay circuit are not in series between the pad 110 and a transistor. *See* Figure 2 of the '602 reference. Accordingly, the '602 reference fails to teach a time-delay circuit including a resistor and a capacitive device connected in series as claimed. Therefore, the asserted combination of references lacks correspondence and the § 103(a) rejections based on the '283 and '602 references are improper. Applicant requests that they be withdrawn.

Applicant respectfully traverses the § 103(a) rejections based on the cited John '511 reference. The '511 reference, either alone or in combination with the other cited references, lacks correspondence to the claimed invention. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.*, a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. Because none of the cited references teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. The Examiner's only possible interpretation of this asserted prior art would be an improper rearrangement of their devices for different functions. As such, the rejections fail.

More specifically, the Office Action acknowledges that the '511 reference does not teach or suggest a time-delay circuit that includes a resistor and a capacitive device connected as in the claimed invention (*see, e.g.*, page 8 of the instant Office Action). The '109 reference, however, also fails to teach such a time-delay circuit. Specifically, the '109 reference does not teach that resistor 44 (or resistor 46) is connected in series with capacitor 42 (*i.e.*, the asserted capacitive device) between terminal VDD and the control inputs of transistors 28 and 30 as is shown in Figure 11. Instead, Figure 11 shows the

asserted resistors 44 and 46 as being in parallel with the asserted capacitive device 42. As such, the Office Action fails to cite any reference that teaches the time-delay circuit of the claimed invention.

Moreover, the '511 reference expressly teaches away from the asserted combination with the '109 reference. *See, e.g., KSR* discussed above. Further, “[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.” M.P.E.P. § 2143.01. The '511 reference is directed to an ESD protection circuit which avoids false triggering without high-speed digital circuitry. The principle of operation of the '511 reference is that the “ESD detector does not include capacitors for sensing of the ESD event thus is not susceptible to false triggering when used in high-speed digital circuitry.” Col. 2:14-17. In attempting to establish a *prima facie* case of obviousness, the Office Action proposes adding the MOS gate 42 capacitor of the '109 reference, which is expressly taught by the '109 reference to be a capacitor (*see, e.g.,* Figures 4 and 11 and Col. 9:60-67), to the ESD detector of the '511 reference. This is directly contrary to the '511 reference’s express principle of operation to avoid the use of capacitors in order to limit the amount of false triggering. In addition, this is one of the primary objects of the '511 reference and the proposed modification would render the circuit of the '511 reference unsuitable for use in high-speed digital circuitry. *See, e.g.,* M.P.E.P. § 2143.01 (“If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.”). Accordingly, the § 103(a) rejections based on the '511 reference are improper and Applicant requests that they be withdrawn.

Applicant respectfully renewes the traversal of the objection to the drawings because the objection relies upon an improper interpretation of the U.S.P.T.O. rules. Specifically, the Office Action erroneously asserts that the drawings “must show every feature of the invention specified in the claims.” The definition of a feature is a prominent attribute or aspect of something. In this instance, the specific aspects identified as missing (*i.e.,* a parasitic npn transistor and a thyristor), while possibly

relevant, are not prominent attributes or aspects. Rather than limit the cited rule (37 C.F.R. § 1.83(a)) to prominent aspects of the claims, the Office Action appears to take the position that the figures must provide a near word-for-word correspondence to the claims. In response to Applicant's previous arguments the Office Action simply reiterates that the objection "is for the claimed elements . . . not shown in the drawings, not for the details not shown as described in the specification." This does not address Applicant's argument regarding the interpretation of 37 C.F.R. § 1.83(a) with respect to a feature being a prominent attribute or aspect of something. Nor does it respond to the specific arguments, reproduced below, regarding the requirements of specifics to support Applicant's position.

The Office Action's apparent interpretation of 37 CFR § 1.83(a) is contrary to the U.S.P.T.O. practice, U.S. law and the M.P.E.P. In support of Applicant's position reference is made to 35 USC § 113 and M.P.E.P. § 601.01(f), which indicate that "applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented." The authority for the U.S.P.T.O. to create rules such as 37 C.F.R. § 1.83(a) is derived from 35 USC § 113. Accordingly, 37 C.F.R. § 1.83(a) must be interpreted in light of this law to ensure that the U.S.P.T.O. does not exceed the statutory authority granted by the U.S. Congress. Moreover, M.P.E.P. § 608.02(e) clarifies how 37 C.F.R. § 1.83(a) should be interpreted and applied by an examiner: "The drawings are objected to under 37 CFR 1.83(a) because they fail to show [1] as described in the specification. Any structural detail *that is essential for a proper understanding of the disclosed invention* should be shown in the drawing." (*emphasis added*). This language is the suggested paragraph for an examiner that wishes to use a 37 C.F.R. § 1.83(a) objection. The Office Action has not used this language, choosing instead to ignore the second half of the suggested language. Accordingly, the objection to the drawings is improper and must be withdrawn.

Regarding the objection to the specification, Applicant re-asserts that any explanation/support for the time delay circuit has been provided. In responding to Applicant's previous arguments, the Examiner acknowledges that the time delay circuit includes resistor R and capacitive device MN1. The Examiner also acknowledges that the Specification discusses these devices. Further, R and MN1 are clearly shown as

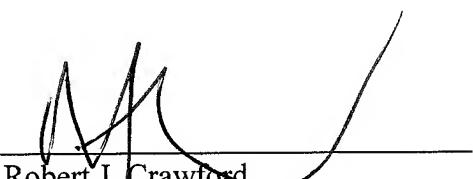
connected to the rest of the circuit in Figure 2, which is part of the specification. As such, it is unclear to Applicant upon what basis the Office Action has maintained the objection to Applicant's specification.

Further, the Examiner's assertion that the time delay circuit's affect on the circuit operation be discussed when the specific operation of the circuit is discussed (Office Action page 14) does not appear to be a proper basis for an objection to the specification. The Examiner's asserted reasoning for the rejection does not appear to have support in the M.P.E.P. *See* M.P.E.P. §§ 608.01-608.01(u). The Examiner's rejection appears to be an attempt to suggest where in the Specification Applicant must discuss each portion of the claimed invention. However, the M.P.E.P. does not require that each and every portion of a circuit be discussed each time the operation of the circuit is discussed. Rather, the specification as a whole must disclose all claimed aspects of the invention. To the extent that the Examiner is having trouble understanding the affect of the resistor and capacitive device on the circuit operation, and notwithstanding the above, Applicant would request that the Examiner articulate what Examiner believes to be missing so that Applicant can accurately respond if necessary.

In view of the above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

By: 
Robert J. Crawford
Reg. No. 32,122
(NXPS.446PA)

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